

**AUDIO CELLULAR MATRIX**

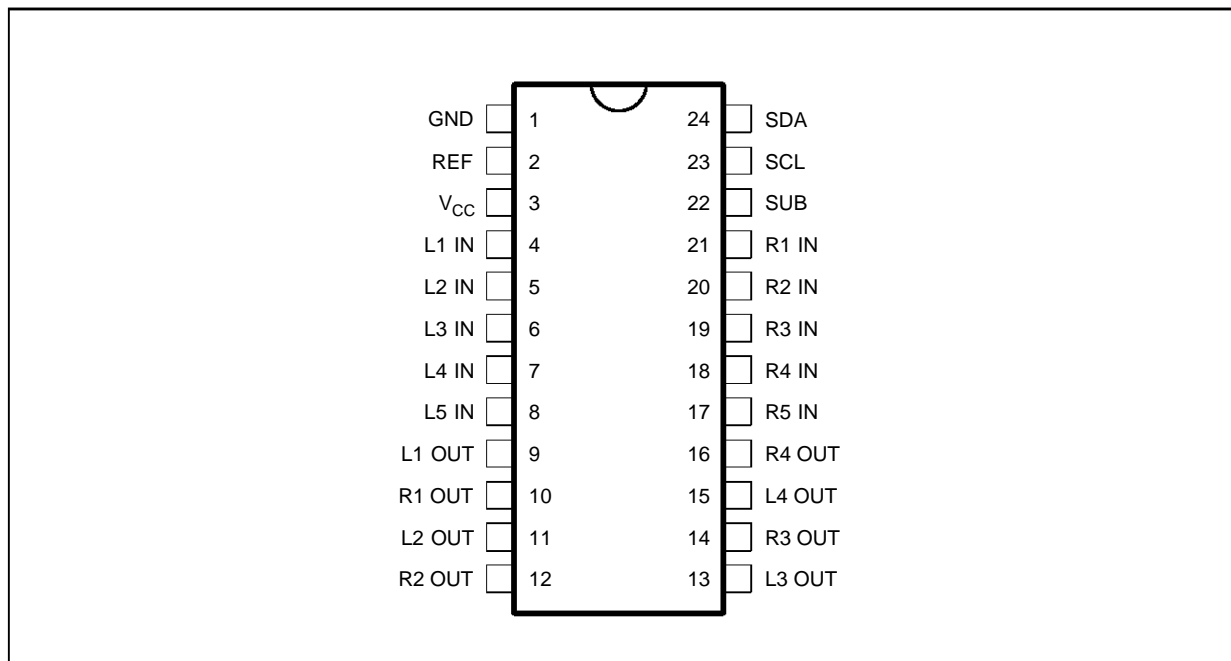
- 5 STEREO INPUTS - 4 STEREO OUTPUTS
- 3-STATE OPERATION FOR EACH OUTPUT
- GAIN OUTPUT CONTROL  
0dB/2/4/6dB/MUTE FOR EACH
- VERY LOW NOISE AND DISTORTION
- I<sup>2</sup>C BUS CONTROL
- 4 SUB-ADDRESS FACILITY
- 90dB CROSSTALK BETWEEN ANY INPUT AND OUTPUT

**DESCRIPTION**

The TEA6430 switches 5 stereo inputs on 4 stereo outputs, providing the customer with high quality sound (low noise, low distortion). The 4 stereo outputs can be set separately in high impedance state, to enable parallel connection of several devices (up to 4). All functions are controlled through the I<sup>2</sup>C bus.

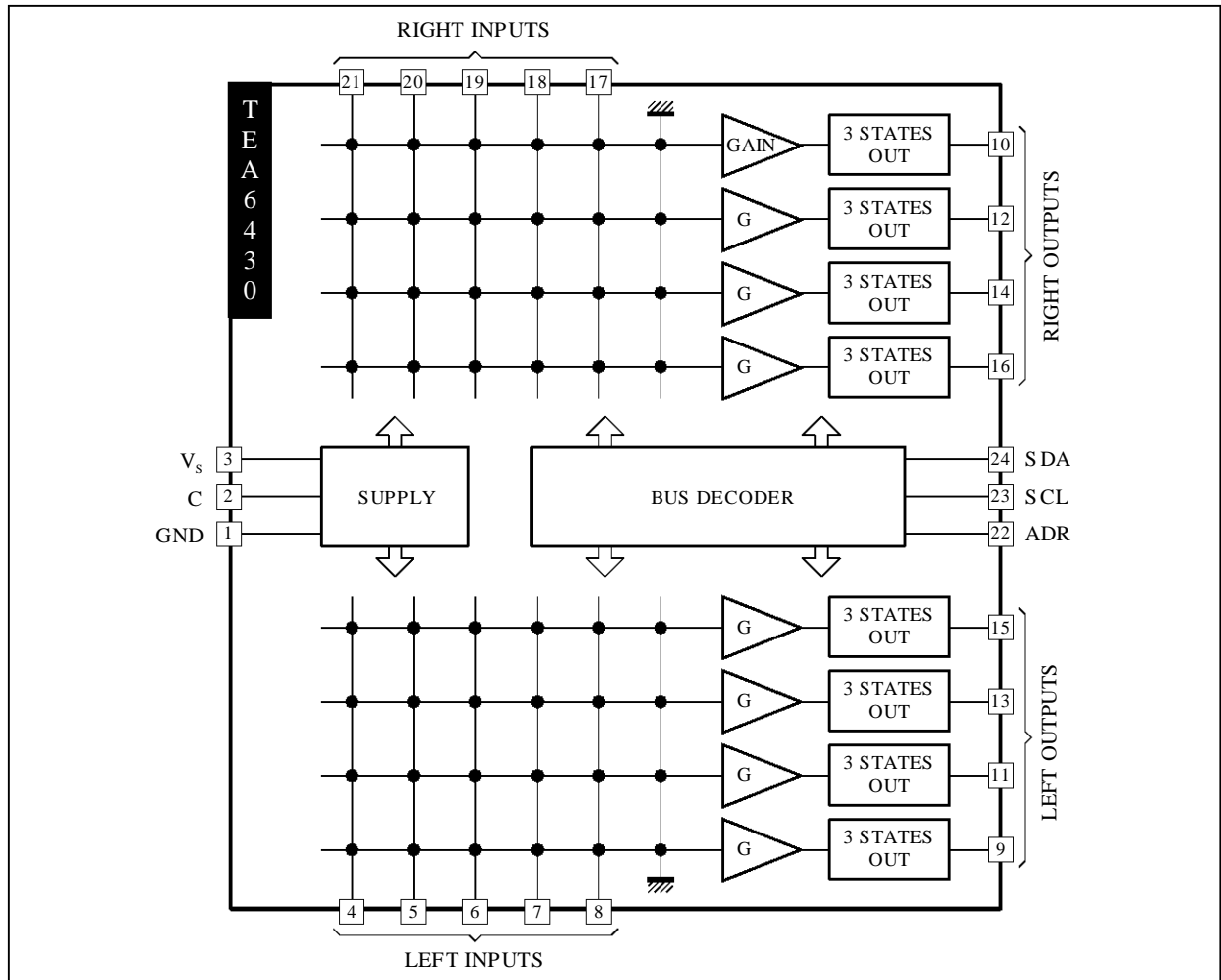


**PIN CONNECTIONS**



6430-01.EPS

BLOCK DIAGRAM



The output loads have to be larger than 2kΩ (typical 10kΩ) and 1500pF

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	12	V
V <sub>I</sub>	Voltage at Pin i to GND	0, V <sub>CC</sub>	V
T <sub>oper</sub>	Operating Ambient Temperature	0, + 70	°C
T <sub>stg</sub>	Storage Temperature	-20, + 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
R <sub>th(j-a)</sub>	Junction-ambient Thermal Resistance	75	°C/W

**ELECTRICAL CHARACTERISTICS**

( $V_{CC} = 8V$ ,  $T_{amb} = 25^{\circ}C$ ,  $R_L = 10k\Omega$ ,  $R_G = 600\Omega$ ,  $f = 1kHz$ ,  $G = 0dB$ ,  $V_{IN} = 0.5V_{RMS}$  ;  
3-state is controlled by I<sup>2</sup>C bus, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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**SUPPLY**

$V_{CC}$	Supply Voltage		7.2	8	10.2	V
$I_{CC}$	Supply Current		4	7	10	mA
RR	Ripple Rejection	$V_{IN} = 0.5V_{RMS}$ , $f = 1kHz$	70			dB

**AUDIO INPUTS**

$V_{IN}$	Max. Signal Amplitude		2			$V_{RMS}$
$V_{DC}$	Input DC Level			$V_{CC}/2$		V
$R_I$	Input Resistance		30	50	100	k $\Omega$

**AUDIO OUTPUTS**

$R_{OUT}$	Output Resistance			60	100	$\Omega$
$Z_{HI}$	Output "off" Impedance	$f = 20kHz$ , output disabled	50			k $\Omega$
$V_{OFF}$	DC Offset Change	Switching between inputs, see note 1		0.1	5	mV
$V_{OUT}$	Output DC Level		$0.4 V_{CC}$	$V_{CC}/2$	$0.6 V_{CC}$	V
$V_N$	Output Noise Voltage	$B = 20-20kHz$ , flat, see note 2		2.5		$\mu V$
G	Gain	$B = 20-20kHz$ , $R_L = 2k\Omega$	-0.5	0	+0.5	dB
	Isolation "off" State	$f = 1kHz$ , output disabled	85			dB
THD	Distortion	$V_{IN} = 1V_{RMS}$ , $f = 1kHz$		0.01	0.05	%
$V_{CL}$	Clipping Level	$d = 0.3\%$	2	2.3		$V_{RMS}$
$C_S$	L, R Channel Separation	$f = 1kHz$	-85			dB
	Crosstalk Audio Channels	$f = 1kHz$ , see note 3	-85	-100		dB
$C_L$	Load Capacitance		1500			pF

- Notes :
1. DC offset change is less than maximum limit, in all configurations (one or several devices in parallel), provided that the reference Pins (P2) are all connected together.
  2. Flat filter according to CCIR-468-4,  $B = 20Hz-20kHz$
  3. Measured from any selected output which contains no signal to a set of other outputs.

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I<sup>2</sup>C BUS CHARACTERISTICS

Symbol	Parameter	Test Conditions	Standard Mode		Fast Mode		Unit
			Min.	Max.	Min.	Max.	

SCL

V <sub>IL</sub>	Low Level Input Voltage		- 0.3	+ 1.5	- 0.3	+ 1.5	V
V <sub>IH</sub>	High Level Input Voltage		3.0	V <sub>CC</sub> + 0.5	3.0	V <sub>CC</sub> + 0.5	V
I <sub>LI</sub>	Input Leakage Current	V <sub>I</sub> = 0 to V <sub>DD</sub>	- 10	+ 10	- 10	+ 10	μA
f <sub>SCL</sub>	Clock Frequency		0	100	0	400	kHz
t <sub>R</sub>	Input Rise Time	1.5V to 3V		1000		300	ns
t <sub>F</sub>	Input Fall Time	1.5V to 3V		300		300	ns
C <sub>I</sub>	Input Capacitance			10		10	pF

SDA

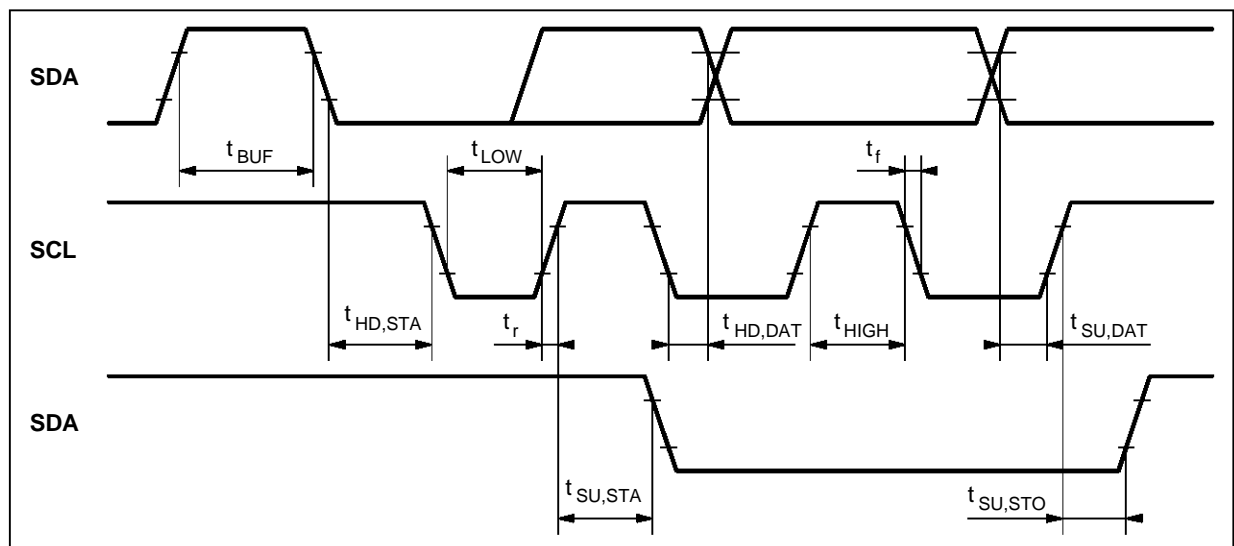
V <sub>IL</sub>	Low Level Input Voltage		- 0.3	+ 1.5	- 0.3	+ 1.5	V
V <sub>IH</sub>	High Level Input Voltage		3.0	V <sub>CC</sub> + 0.5	3.0	V <sub>CC</sub> + 0.5	V
I <sub>LI</sub>	Input Leakage Current	V <sub>I</sub> = 0 to V <sub>DD</sub>	- 10	+ 10	- 10	+ 10	μA
C <sub>I</sub>	Input Capacitance			10		10	pF
t <sub>R</sub>	Input Rise Time	1.5V to 3V		1000		300	ns
t <sub>F</sub>	Input Fall Time	1.5V to 3V		300		300	ns
V <sub>OL</sub>	Low Level Output Voltage	I <sub>OL</sub> = 3mA		0.4		0.4	V
t <sub>F</sub>	Output Fall Time	3V to 1.5V		250		250	ns
C <sub>L</sub>	Load Capacitance			400		400	pF

TIMING

t <sub>LOW</sub>	Clock Low Period		4.7		1.3		ms
t <sub>HIGH</sub>	Clock High Period		4.0		0.6		ms
t <sub>SU, DAT</sub>	Data Set-up Time		250		100		ns
t <sub>HD, DAT</sub>	Data Hold Time		0	340	0	340	ns
t <sub>SU, STO</sub>	Set-up Time from Clock High to Stop		4.0		0.6		μs
t <sub>BUF</sub>	Start Set-up Time following a Stop		4.7		1.3		μs
t <sub>HD, STA</sub>	Start Hold Time		4.0		0.6		μs
t <sub>SU, STA</sub>	Start Set-up Time following Clock Low-to-High Transition		4.7		0.6		μs

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Figure 1 : I<sup>2</sup>C Bus Timing



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## I<sup>2</sup>C BUS SELECTION

### I<sup>2</sup>C Bus Slave Address

Address	A6	A5	A4	A3	A2	A1	A0	R/W
Value	1	0	0	1	1	A1	A0	0

### Sub-address I<sup>2</sup>C

Symbol	Parameter	Conditions	Pin 22 Voltage (typ.)	Unit
Vsub	Slave address HEXA	Sub-address (see note)		
1	98	A1    A0 0    0	GND	V
2	9E	1    1	V <sub>CC</sub>	V
3	9C	1    0	1/3	V <sub>CC</sub>
4	9A	0    1	2/3	V <sub>CC</sub>

**Note :** The first 3 levels are defined by connecting the sub-address pin to the appropriate level. Sub-address 4 will be selected when this pin is left open.

### Data Byte

	b7	b6	b5	b4	b3	b2	b1	b0	Action
	T	01	00	G1	G0	I2	I1	I0	
Input Select	*	*	*	*	*	0	0	0	IN1
	*	*	*	*	*	0	0	1	IN2
	*	*	*	*	*	0	1	0	IN3
	*	*	*	*	*	0	1	1	IN4
	*	*	*	*	*	1	0	0	IN5
	*	*	*	*	*	1	0	1	Mute
Output Select	*	0	0	*	*	*	*	*	OUT1
	*	0	1	*	*	*	*	*	OUT2
	*	1	0	*	*	*	*	*	OUT3
	*	1	1	*	*	*	*	*	OUT4
Gain	*	*	*	0	0	*	*	*	6dB
	*	*	*	0	1	*	*	*	4dB
	*	*	*	1	0	*	*	*	2dB
	*	*	*	1	1	*	*	*	0dB
Tri-state	0	*	*	*	*	*	*	*	Low impedance Tri-state
	1	*	*	*	*	*	*	*	

**Example :** 00111100 enables L(R)2 out and connect it with a gain of 0dB to L(R)5 in.

### Power On Reset

When active : outputs in 3-state. All outputs are disabled and L(R)5 is selected to drive all outputs. Gain = 0dB.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Reset	Start of Reset	Incr. V <sub>CC</sub>			2.5	V
	End of Reset	Decr. V <sub>CC</sub> Incr. V <sub>CC</sub>	4.5		4.2	V

TYPICAL PERFORMANCES

Figure 1 : Supply Current as a Function of Supply Voltage

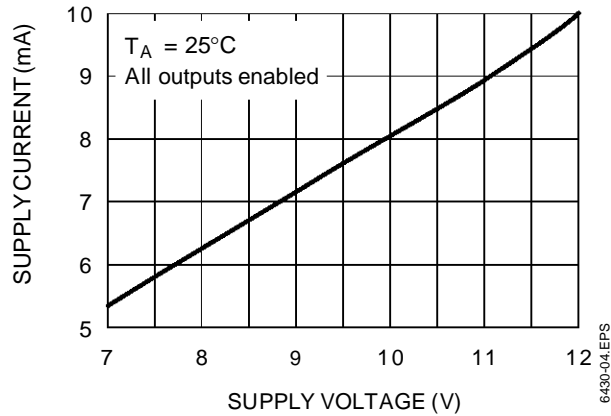


Figure 2 : Supply Current as a Function of Temperature

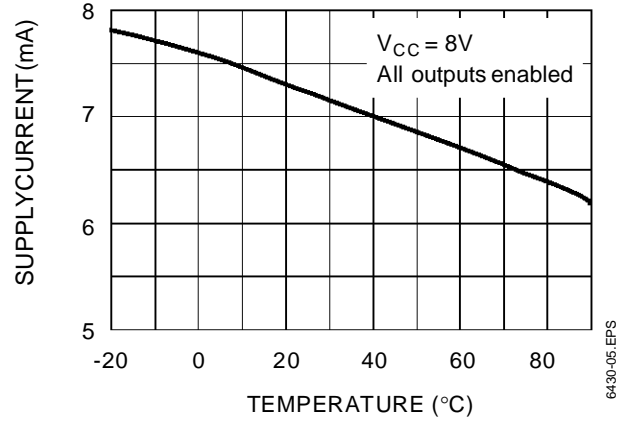


Figure 3 : Ripple Rejection as a Function of Supply Voltage

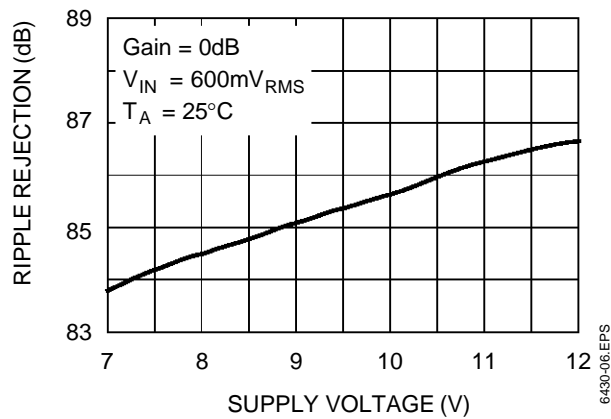


Figure 4 : Ripple Rejection as a Function of Temperature

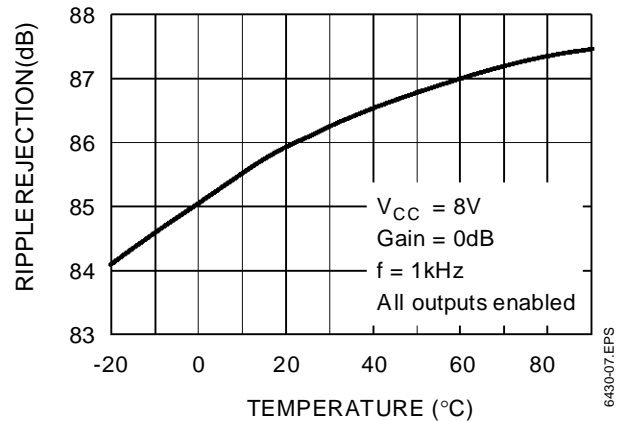


Figure 5 : Ripple Rejection as a Function of Gain

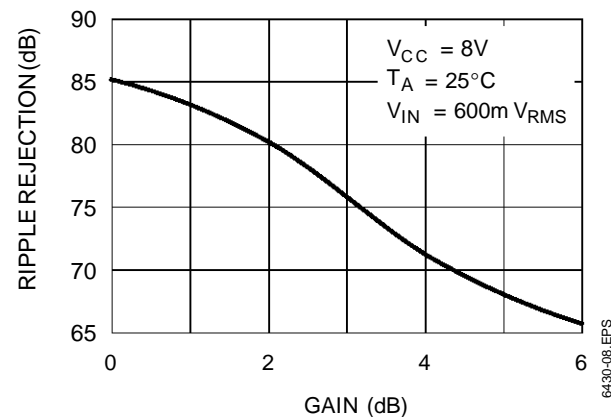
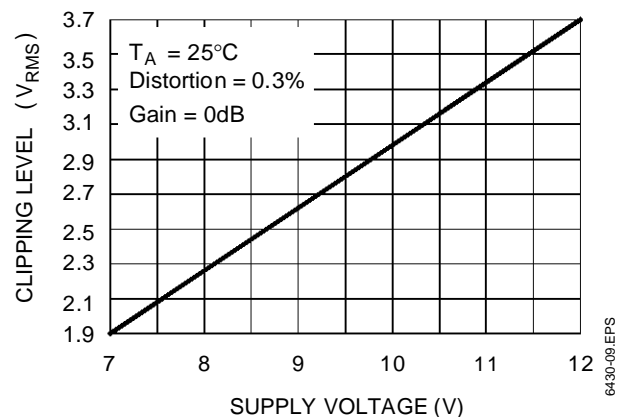


Figure 6 : Clipping Level as a Function of Supply Voltage



TYPICAL PERFORMANCES (continued)

Figure 7 : Distortion as a Function of Input Level

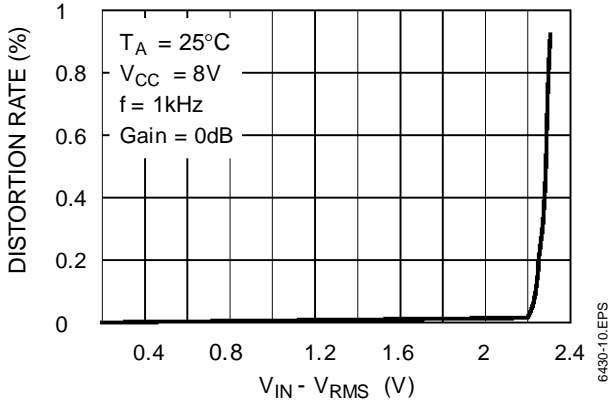


Figure 8 : Distortion as a Function of Gain

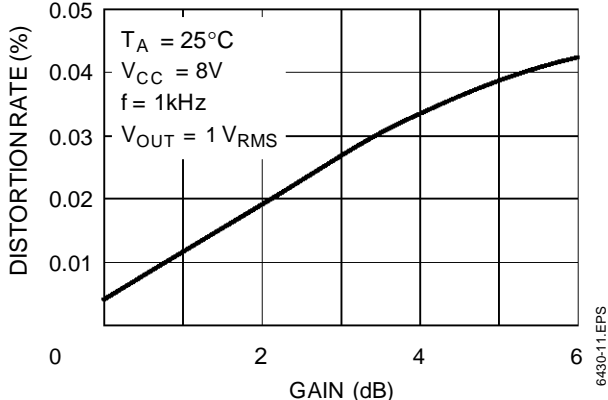


Figure 9 : Crosstalk Level as a Function of Frequency (Gain = 0dB)

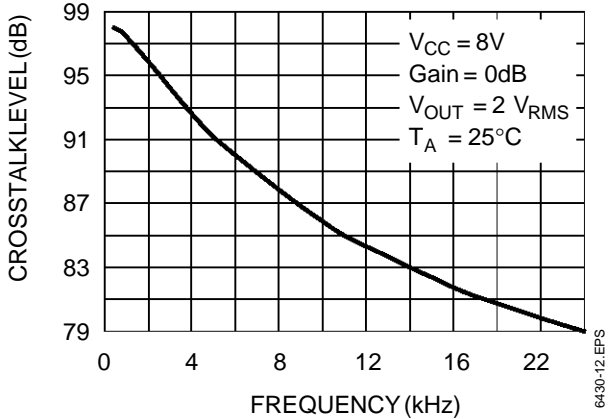
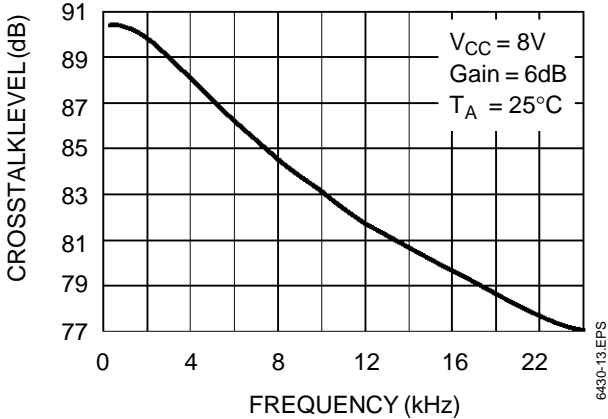


Figure 10 : Crosstalk Level as a Function of Frequency (Gain = 6dB)



PIN CONFIGURATIONS

Figure 11 : Audio IN

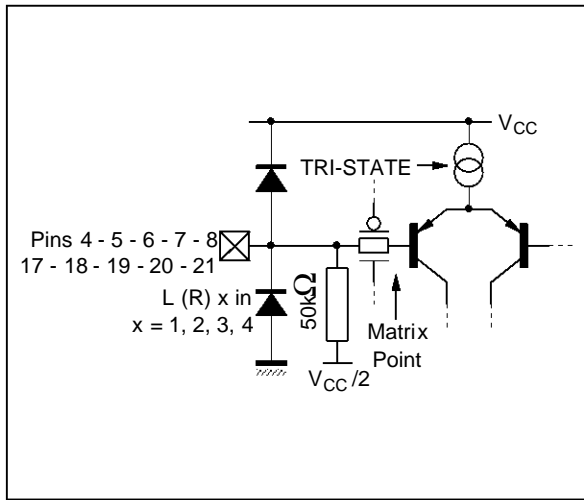


Figure 12 : Audio OUT

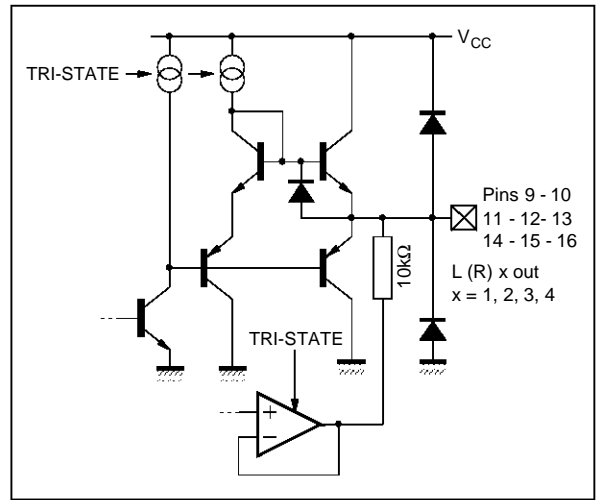


Figure 13 : PROG

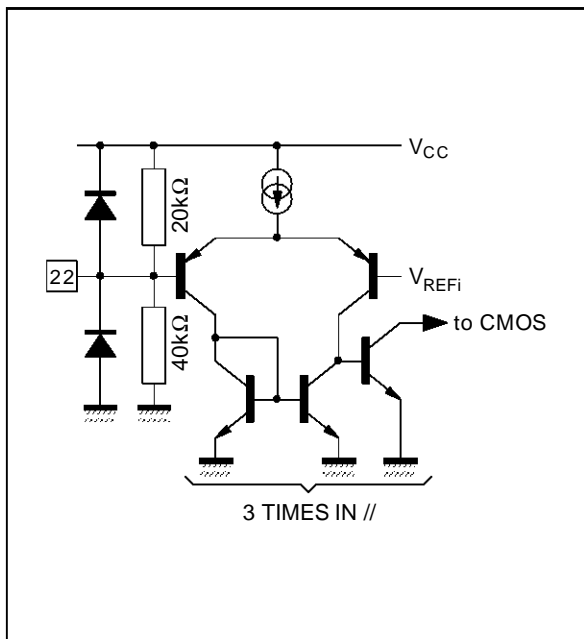
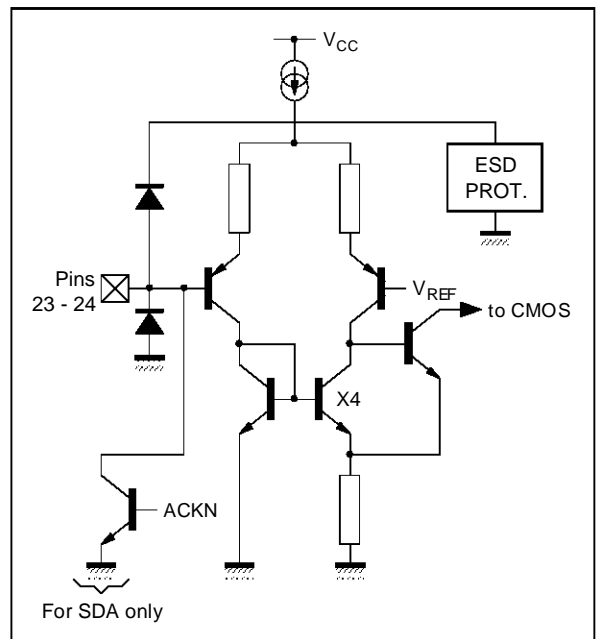
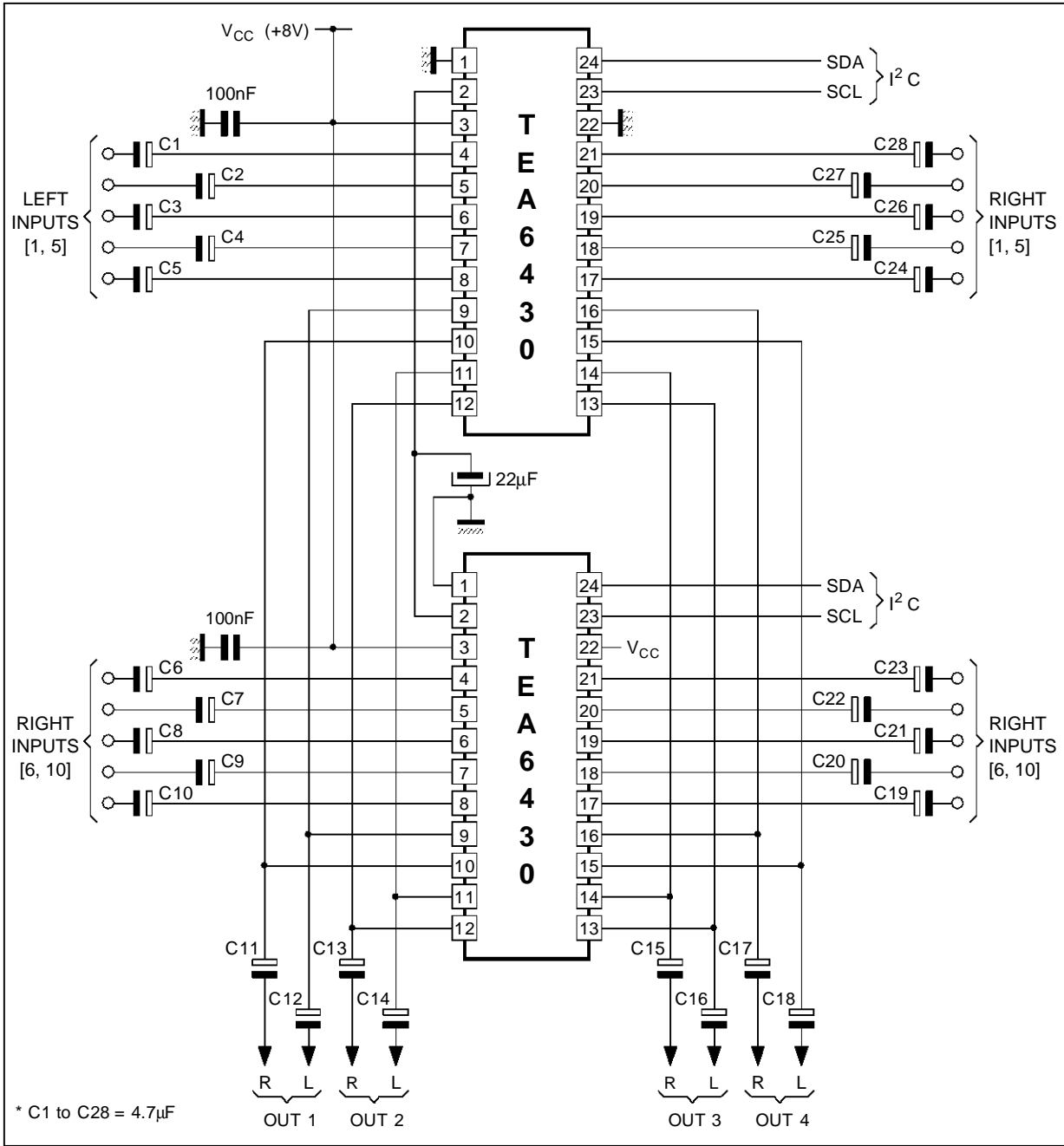


Figure 14 : Bus Inputs



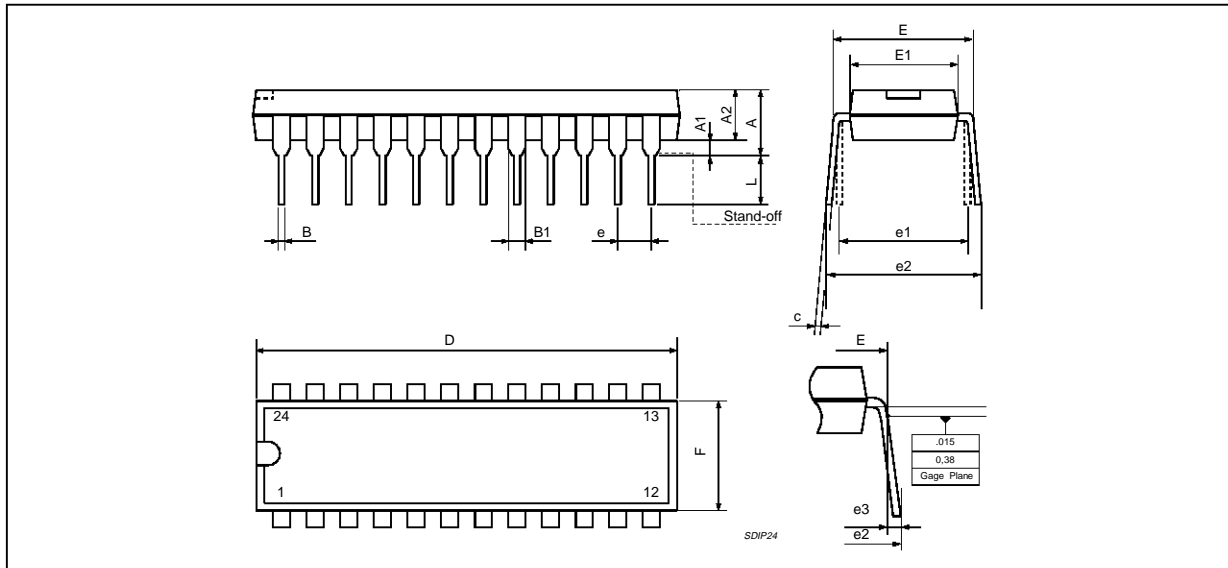


TYPICAL APPLICATION



6430-18.EPS

**PACKAGE MECHANICAL DATA**  
24 PINS - PLASTIC SHRINK DIP



PMSDIP24LEPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.30	4.57	0.120	0.130	0.180
B	0.36	0.46	0.56	0.0142	0.0181	0.0220
B1	0.76	1.02	1.14	0.030	0.040	0.045
C	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	22.61	22.86	23.11	0.890	0.90	0.910
E	7.62		8.64	0.30		0.340
E1	6.10	6.40	6.86	0.240	0.252	0.270
e		1.778			0.070	
e1		7.62			0.30	
e2			10.92			0.430
e3			1.52			0.060
L	2.54	3.30	3.81	0.10	0.130	0.150

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